Abstract Of The Invention

An SOC architecture that provides a latency tolerant protocol for internal bus signals is disclosed. The SOC includes at least a processor core and one or more peripherals that communicate on a first internal bus that carries signals having a latency tolerant signal protocol that enables an arbitrary number of pipeline stages between any signal initiator and any signal target. A shared memory subsystem, DMA-type peripherals, and a second internal bus with a topology overlapping the first bus, may also be included. All signals over both busses are point-to-point and registered and all transactions on both busses are handshaked. An arbitrary number of flip-flops, multiplexing routers, and/or decoding routers may be included between any signal initiator and any signal target on either bus, and may be added at any time during the design and layout of the SOC.